Resource Descriptions

The S(o)OS Consortium

January 26, 2012

Introduction

Purposes of a Resource Description:

- Modeling
- Simulation
- Synthesis
- Code adaptation
- Segmentation
- Mapping
- Scheduling
- Compiler generation
- etc.

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Type of information

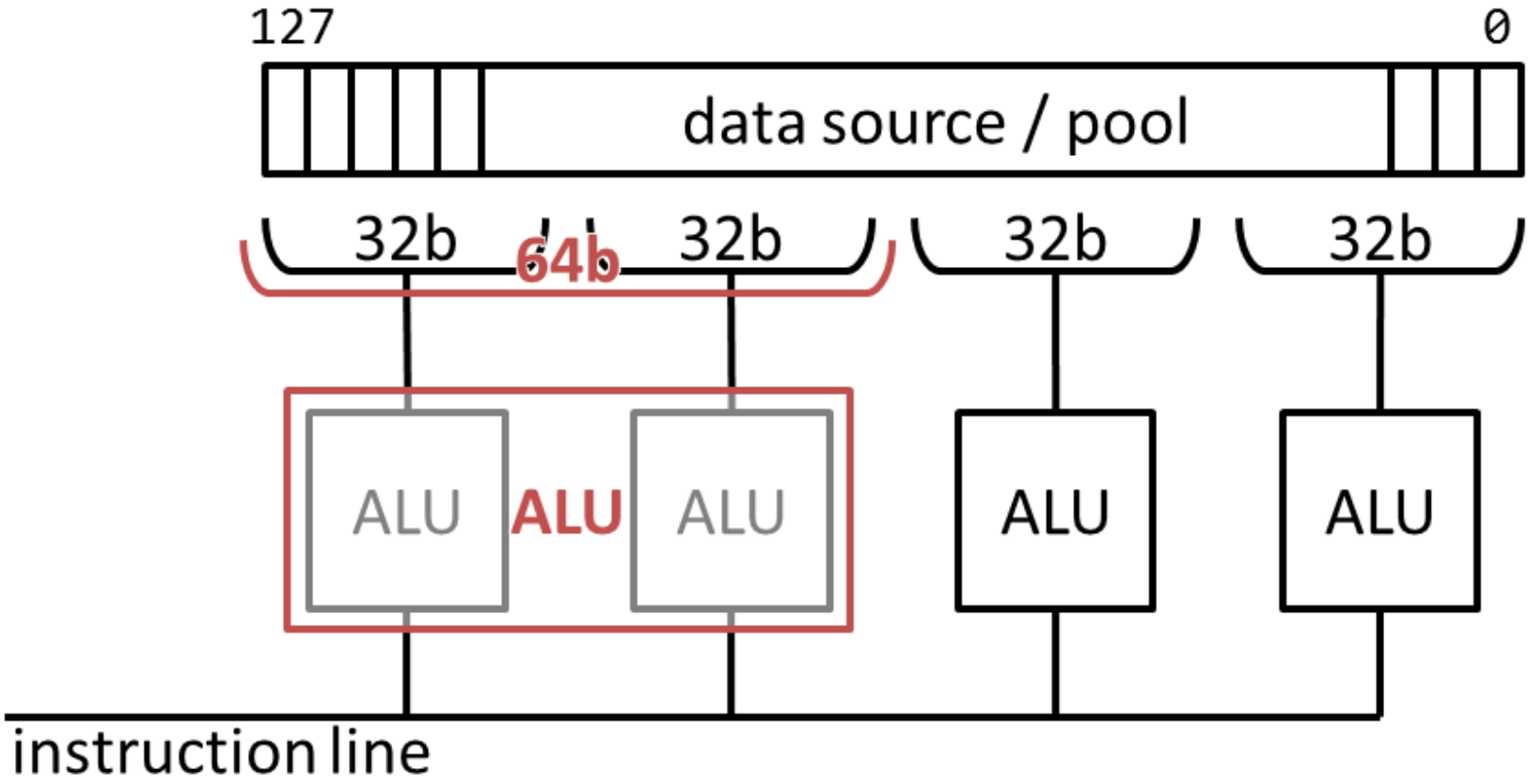
What type of information do we want to store:

- Type of core
- Memory map
- Latency
- Connectivity
- ISA
- etc.

Small Example

```
dlx = machine hierarchy (dlxPU il il)                                  1
  where                                                                2
    mem = [pmem, dmem]                                                 3
      where                                                            4
        pmem = ProgMem "pmem"                                          5
               (0 x0000000, 0 x00FFFFF) 1 (0 x0, 0 xFFFFF)             6
        dmem = DataMem "dmem"                                          7
               (0 x0100000, 0 x01FFFFF) 1 (0 x0, 0 xFFFFF)             8
    l1        = cacheDM size lineSize hitStrat misStrat latency        9
    l2        = cacheSA A2W 256 1 RAND WT WAR 3                        10
    hierarchy = l1 `bindsToCache` l2 `bindsHToMem` mem                 11
    il        = IL "dlxOPC"                                            12
```

Small Example



Small Example

```
dlxPU il0 il1 = PU {alus = [alu0, alu1], registers = [reg0]}
  where
    alu0  = ALU {function = "ADD, MUL", aluType = "FP"
                , register = reg0, dl = dl0, il = il0}
    alu1  = ALU ...
    dl0   = DL {pool = pool0, address = 0, width = 32}
    dl1   = DL {pool = pool0, address = 32, width = 32}
    pool0 = DataPool {size = 64, poolId = "0"}
    reg0  = Register {rId = "0"}
```

PU Analysis

$$\textbf{data}\ \mathit{FlynnCategory} = \mathit{SISD} \mid \mathit{SIMD} \mid \mathit{MISD} \mid \mathit{MIMD} \quad (1)$$

$$\mathit{flynnCategory} :: [\mathit{ALU}] \rightarrow \mathit{FlynnCategory} \quad (2)$$

$$\mathit{flynnCategory}\ [a] = \mathit{SISD} \quad (3)$$

$$\begin{aligned}
\mathit{flynnCategory}\ \mathit{alus} \mid\ & \mathit{sameIL}\ \mathit{alus} \wedge \mathit{dataShared}\ \mathit{alus} && = \mathit{SISD} && (4)\\
\mid\ & \mathit{sameIL}\ \mathit{alus} && = \mathit{SIMD} && (5)\\
\mid\ & \neg\ (\mathit{sameIL}\ \mathit{alus}) \wedge \mathit{dataShared}\ \mathit{alus} && = \mathit{MISD} && (6)\\
\mid\ & \neg\ (\mathit{sameIL}\ \mathit{alus}) \wedge \neg\ (\mathit{dataShared}\ \mathit{alus}) && = \mathit{MIMD} && (7)
\end{aligned}$$

PU Analysis

$$\textbf{data}\ \mathit{FlynnCategory} = \mathit{SISD} \mid \mathit{SIMD} \mid \mathit{MISD} \mid \mathit{MIMD} \quad 1$$

$$\mathit{flynnCategory} :: [\mathit{ALU}] \to \mathit{FlynnCategory} \quad 2$$

$$\mathit{flynnCategory}\ [a] = \mathit{SISD} \quad 3$$

$$\begin{aligned} \mathit{flynnCategory}\ \mathit{alus} \mid\ & \mathit{sameIL}\ \mathit{alus} \wedge \mathit{dataShared}\ \mathit{alus} && = \mathit{SISD} && 4\\ \mid\ & \mathit{sameIL}\ \mathit{alus} && = \mathit{SIMD} && 5\\ \mid\ & \neg\,(\mathit{sameIL}\ \mathit{alus}) \wedge \mathit{dataShared}\ \mathit{alus} && = \mathit{MISD} && 6\\ \mid\ & \neg\,(\mathit{sameIL}\ \mathit{alus}) \wedge \neg\,(\mathit{dataShared}\ \mathit{alus}) && = \mathit{MIMD} && 7 \end{aligned}$$

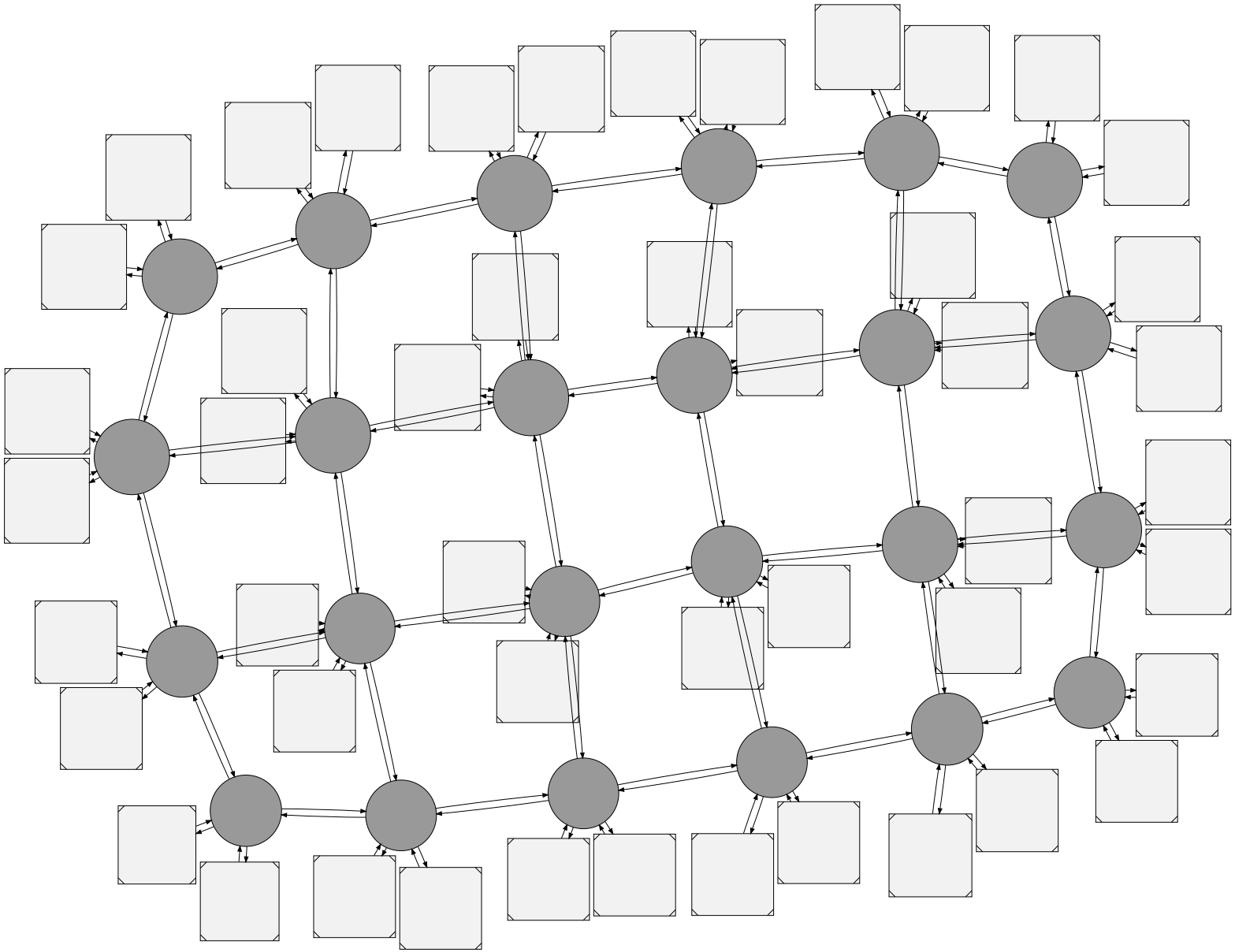
$$\mathit{superscalar} :: \mathit{PU} \to \mathit{Bool} \quad 8$$

$$\begin{aligned} \mathit{superscalar}\ (\mathit{PU}\ \{\mathit{alus} = \mathit{alus}\}) = {} & (\mathit{flynnCategory}\ \mathit{alus} \equiv \mathit{MIMD}) \wedge && 9\\ & \mathit{shareAllRegisters}\ \mathit{alus} && 10 \end{aligned}$$

Networked example

$$
\begin{array}{ll}
\mathit{meshMachine} = \mathit{meshConnect}\ 6\ 4\ \mathit{rlink}\ \mathit{rxbRouter}\ [\mathit{dlx}, \mathit{dlx}] & 1 \\
\quad \textbf{where} & 2 \\
\qquad \mathit{rlink} = \mathit{Link}\ \{\mathit{bandwidth} = 16, \mathit{latency} = 4, \mathit{freq} = 400\} & 3
\end{array}
$$

Networked example



Missing information

What information is not captured by our model:

- Relation between caches (inclusive vs. exclusive)
- NUMA aspects of the memory map