VARIABILITY ASSESSMENT OF 10NM BULK-PLANAR VS FULLY-DEPLETED FINFET SRAM

AUTHORS:

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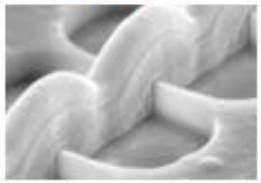
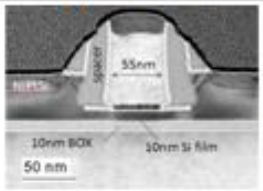
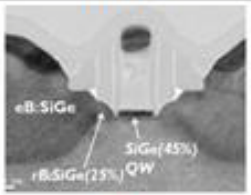
TRAMS WP2 - GENERAL MOTIVATION & OBJECTIVES

Planar CMOS SRAM does not scale well beyond 20nm

Semiconductor industry positions along different alternatives:

- Late CMOS: (Fully depleted) Fin Fet (FF) or mixed (FF & planar), UTBOX SOI
- Post CMOS: III-V (Implant-Free Quantum-Well), CNT,...

	FinFET	UTBox-SOI	IFQW
			
Substrate	Bulk or SOI	SOI (thin Box)	Bulk

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	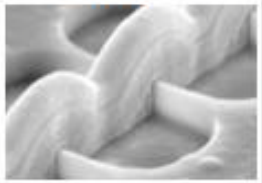	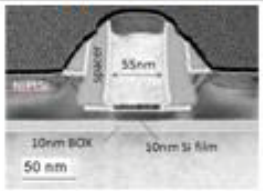	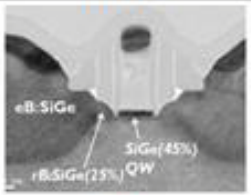
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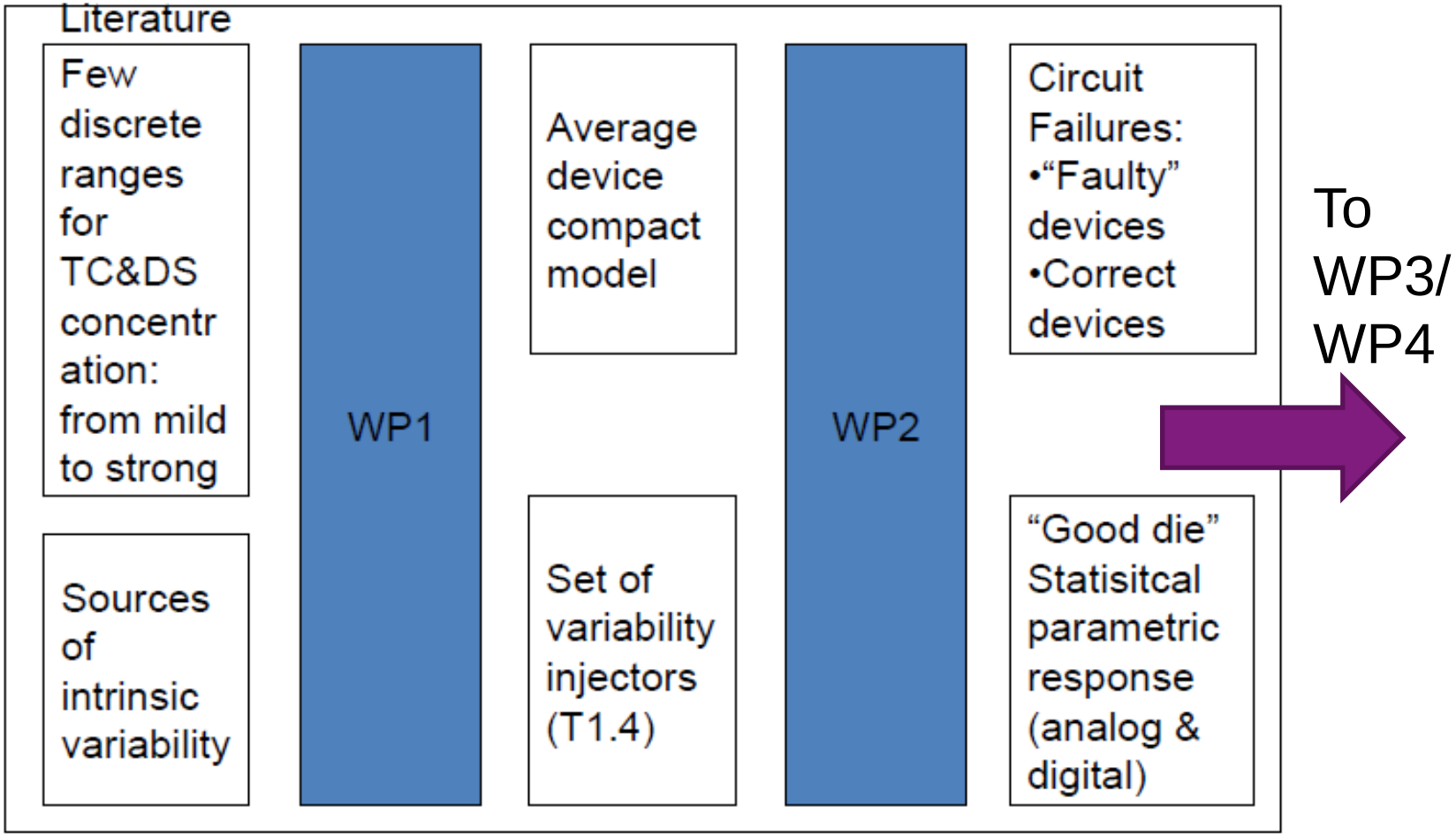
Need to understand advantages of new technologies for SRAM

Examples:

- Tolerable Vccmin?
- Optimal Vt?
- Sensitivity between performance, power, yield for each option?
- ...

PROJECT WIDE POSITIONING



BULK PLANAR VS FIN-FET SRAM: MOTIVATION FOR ASSESSMENT

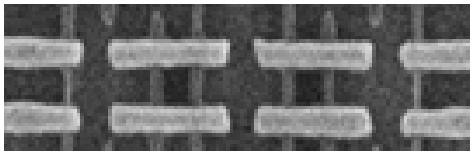
Planar CMOS SRAM V_{CCMIN} does not scale in sub-22nm due to SCE and mismatch sensitivity

FinFET device positions as alternative option to planar

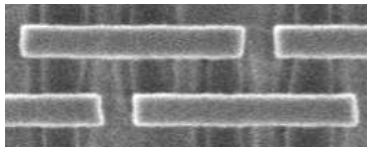
- Better channel control and cell leakage
- Less device variability (less A_{VT})
- Denser than planar?

Objective:

- Understand sensitivities of FoM to technology parameters across abstraction levels



FF-cell (*)



planar-cell(**)

(*) Imec

(**) Courtesy Intel

AGENDA

SRAM SPECS

SRAM DESIGN

STATISTICAL BENCHMARKING

CONCLUSIONS

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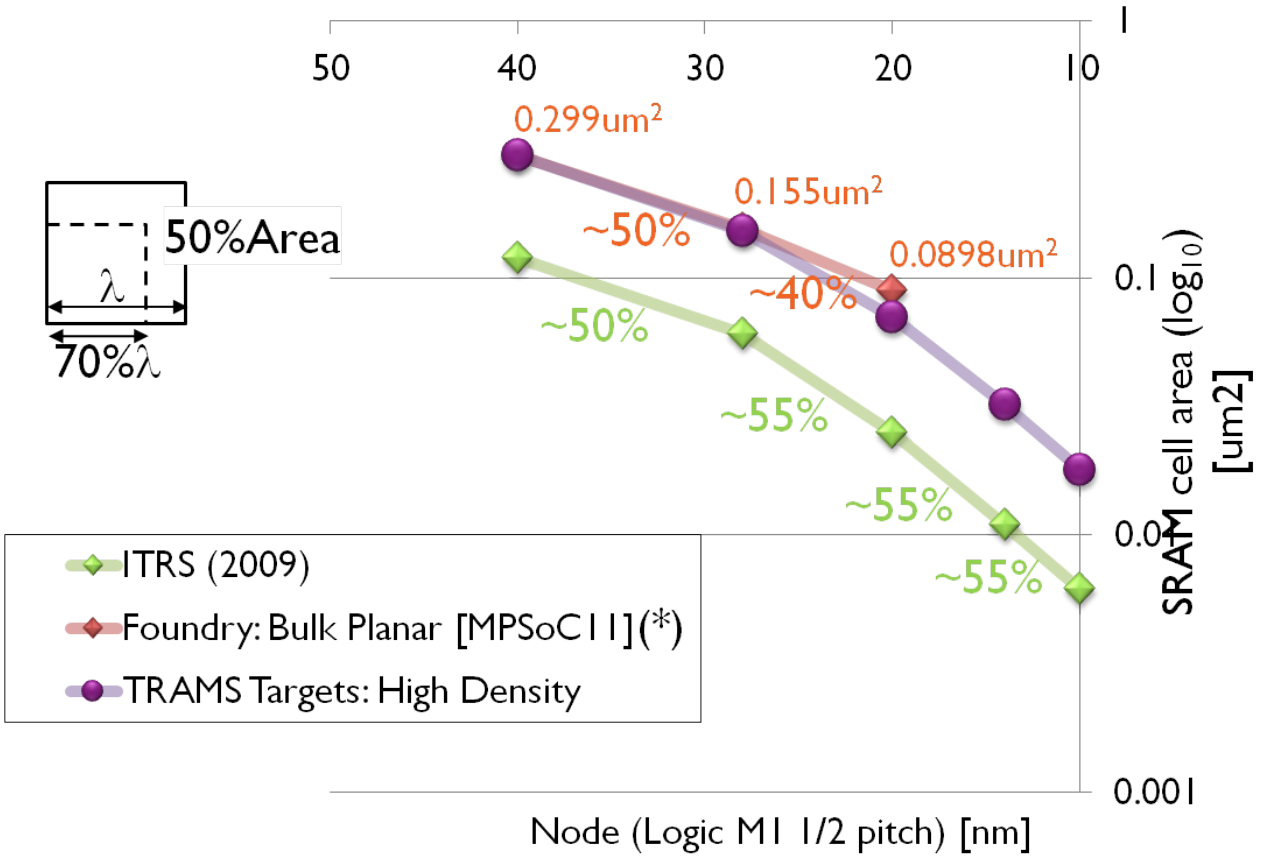
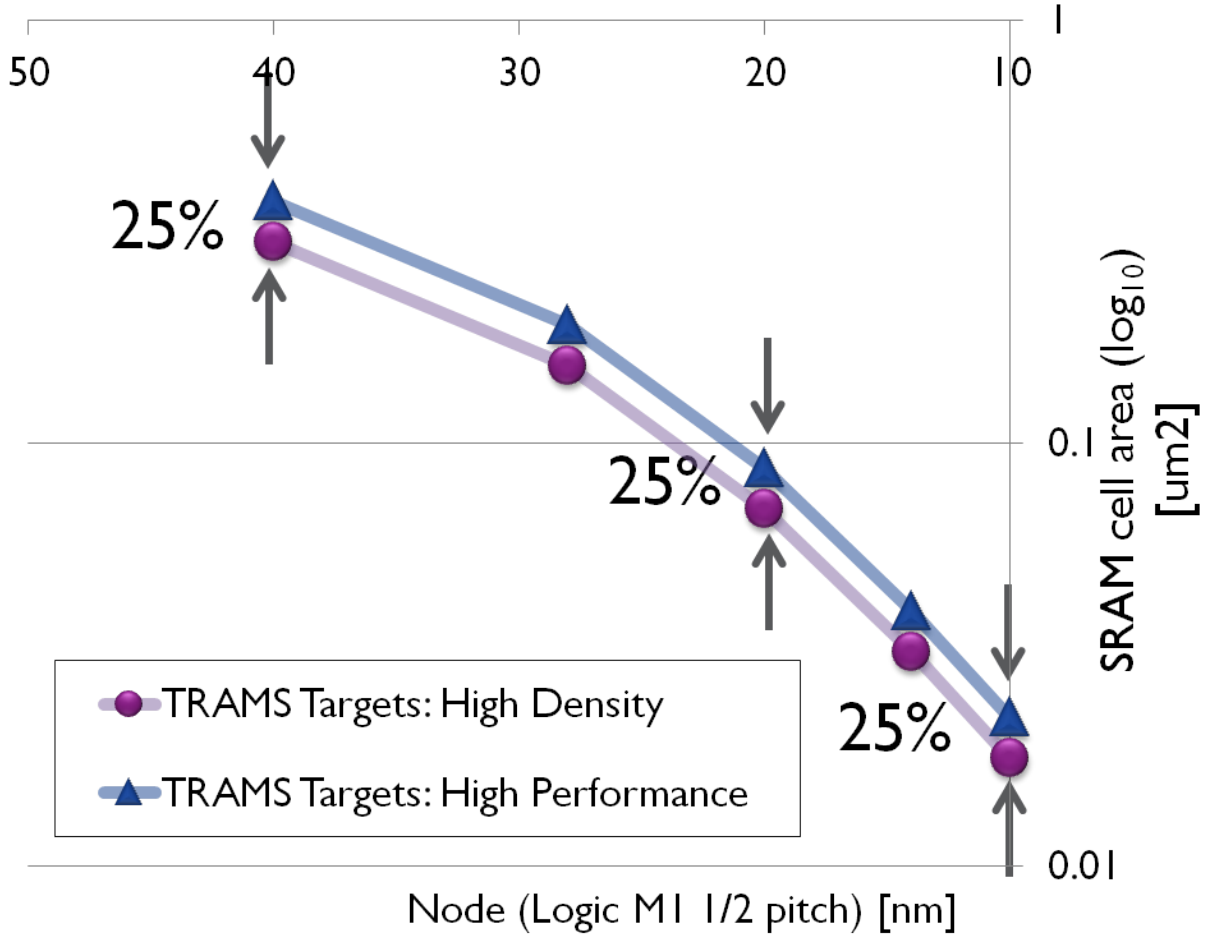
AREA SCALING TRENDS ANALYSIS FOR HIGH DENSITY SRAM FROM 40NM DOWN TO 10NM



(*) B. Sheu, Design Technology for future computing systems, 11th Intl. Forum on Embedded MPSoC & Multicore (Keynote Session 5), May 2011, France

TRAMS TARGETS FOR HIGH PERFORMANCE AND HIGH DENSITY LOW POWER SRAM



ELECTRICAL TARGETS FOR TRAMS'S 10NM SRAM (VDD=0.8V)

	Area	Speed	Power		Stability		Data Ret.
	[um^2]	I_Read [uA]	I_Stby. (Vdd=0.9V) [pA]	I_Sleep (Vdd=0.55V) [pA]	Read SNM (statistical) [mV]	Write SNM (statistical) [mV]	Hold SNM (statistical) [mV]
High Density	0.0187	10	10	1	80	50	50
High Perf.	0.022	30	100	10	80	50	50

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APPROACH

Common Reference Cell architecture

Symbolic Area Analysis

Minimum Area Cell implementation (planar, UTB, BFF)

Area/Vt tuning trade-offs

High Density (planar, UTB, BFF)

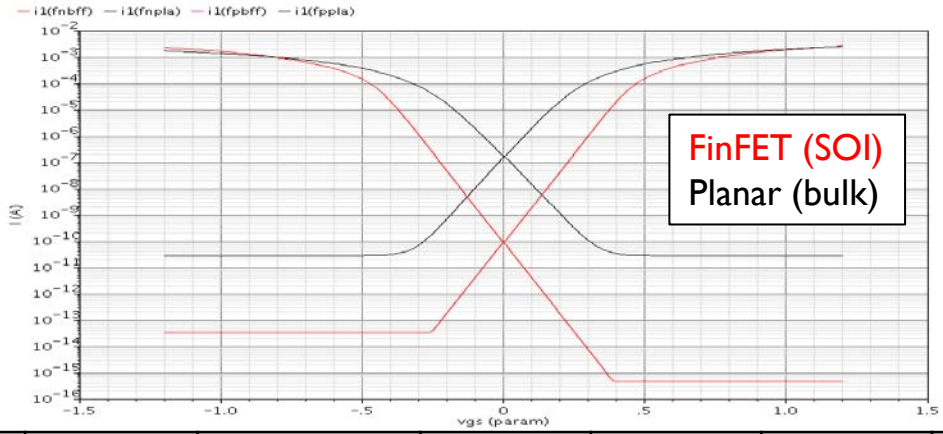
High Performance (planar, UTB, BFF)

STARTING POINT: TRAMS DEVICE MODELS

WP1:

- D1.1: Statistical device model: bulk planar 10nm (UoG)
- D1.2: Statistical device model: FD FF 10nm (UoG)

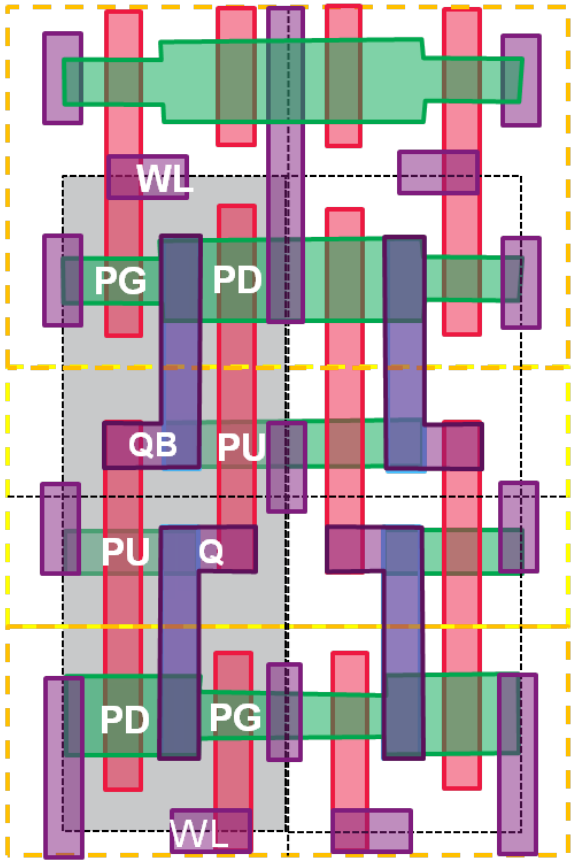
STARTING POINT: DEVICE PERFORMANCE



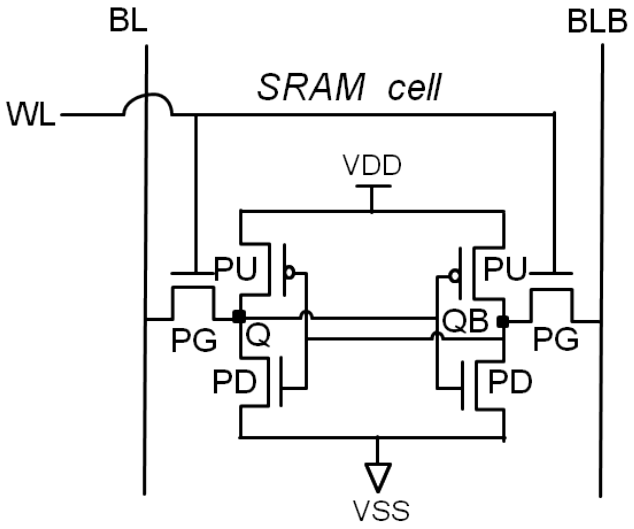
	Unit	Condition	Planar N	Planar P	FinFET N	FinFET P
Vth_lin	mV	Icrit=10uA/um, VDS=50mV	244	-329	411	-414
Vth_sat	mV	Icrit=10uA/um, VDS=VDD	164	-172	374	-373
Vth_sat	mV	Icrit=10uA/um VDS=1V	164	-172	368	-364
S_Slope	mV/dec	-	93.4	-102	76.2	-76.0
DIBL	mV/V	-	85.9	168	49.3	54.7
Ion	uA/um	VDS=VGS=1V	1996	-1340	1938	-1734
Ion	uA/um	VDS=VGD=VDD	1996	-1340	1.133	-973
Ioff	nA/um	VDS=VGS=1V	153	-181	0.129	-0.128
Ioff	nA/um	VDS=VGD=VDD	153	-181	0.0917	-0.0909

SRAM CELL ARCHITECTURE

REFERENCE CELL ARCHITECTURE (*)

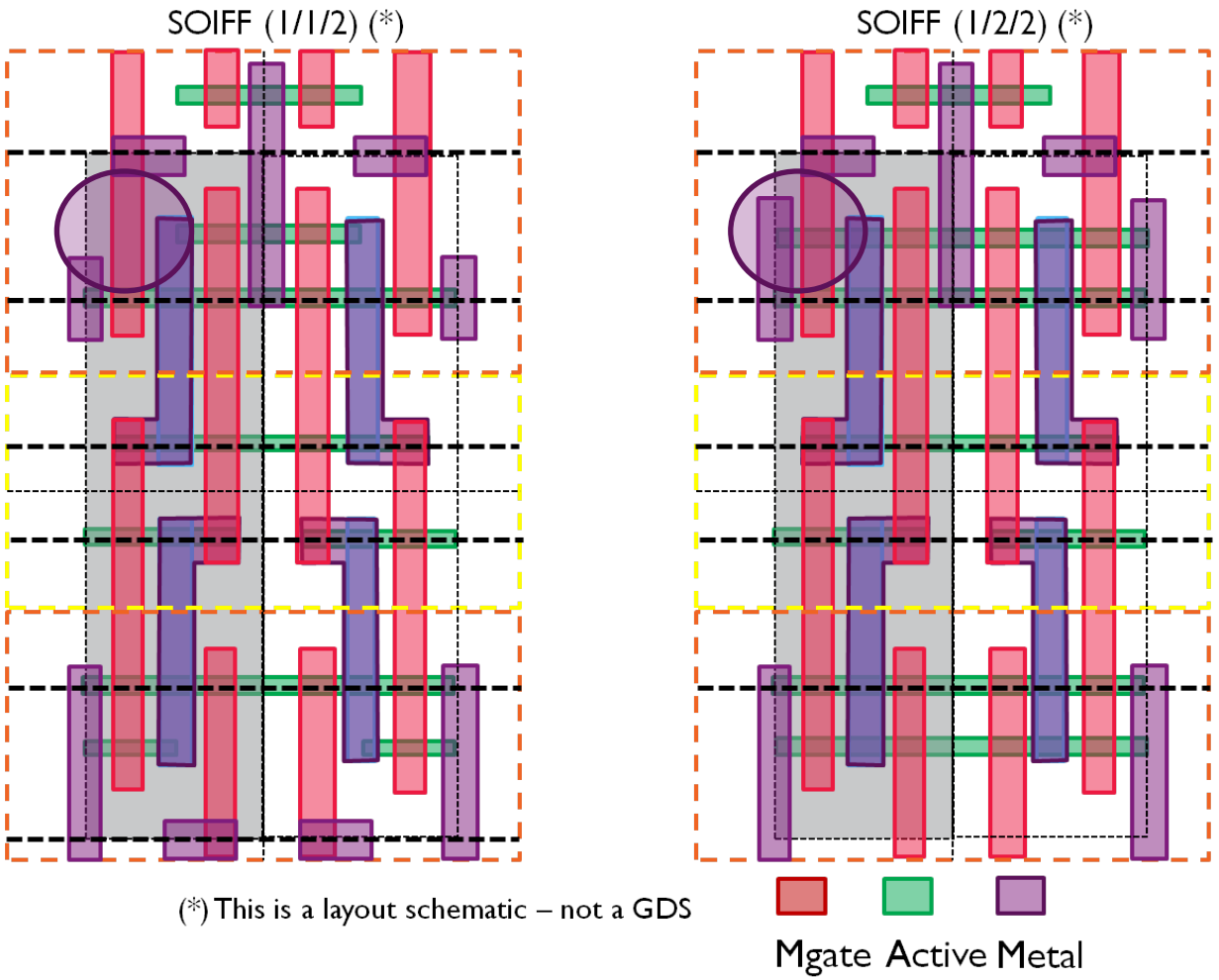


(*) This is a layout schematic – not a GDS

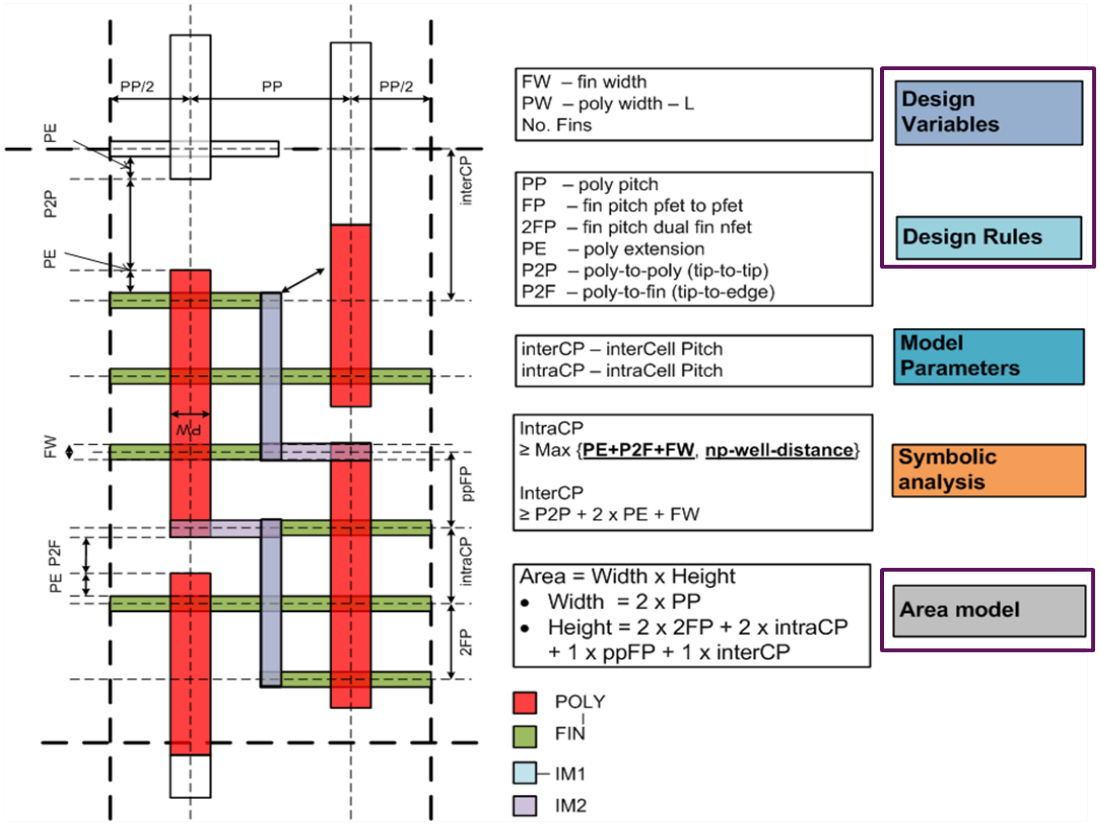


Mgate Active

CELL ARCHITECTURE OPTIONS FOR MLTI-FIN FINFET SRAM CELL CONFIGURATIONS



HIGH-LEVEL AREA MODEL FOR DESIGN EXPLORATION



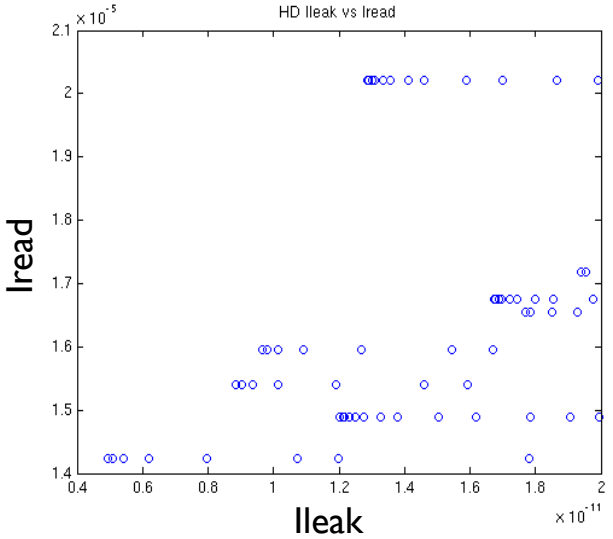
	L [nm]	PDW	PGW	PUW	ΔVtp	ΔVtn
Planar SRAM	13-16	30-45-60	20-35-50	20-27-35	+/- 250	+/- 250

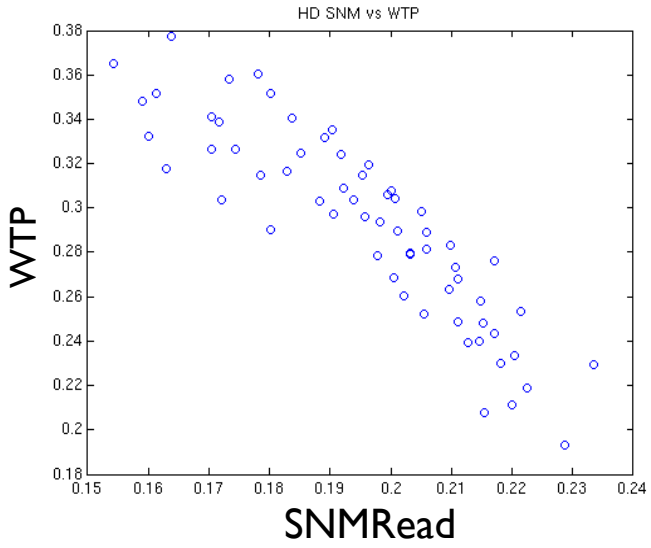
	Fin Lenght	Fin Height	Fin Width	#Fins	ΔVtp	ΔVtn
FinFET SRAM	10	12.5	5	1-3	-100..+200	-200..+100

SRAM CELL DESIGN SPACE: BULK PLANAR CELL (VDD=1.0V)

High Density Low Power (HDLP)

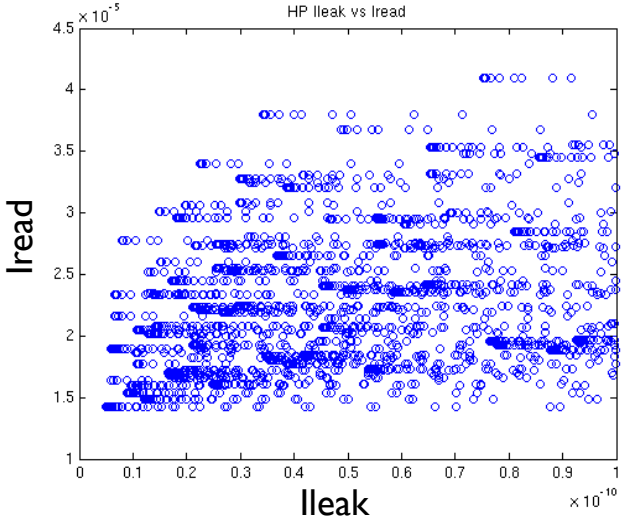
Area < 0.017 um2

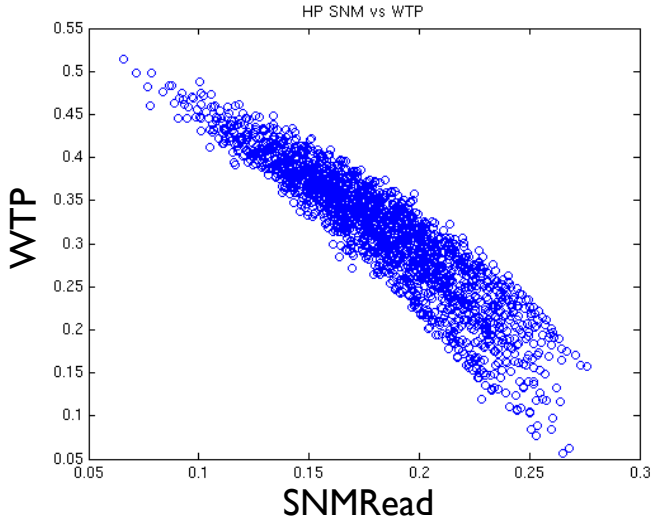




High Performance (HP)

Area < 0.022 um2

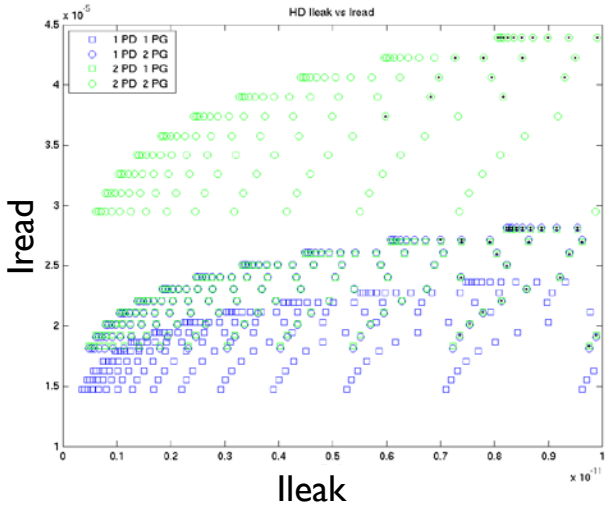


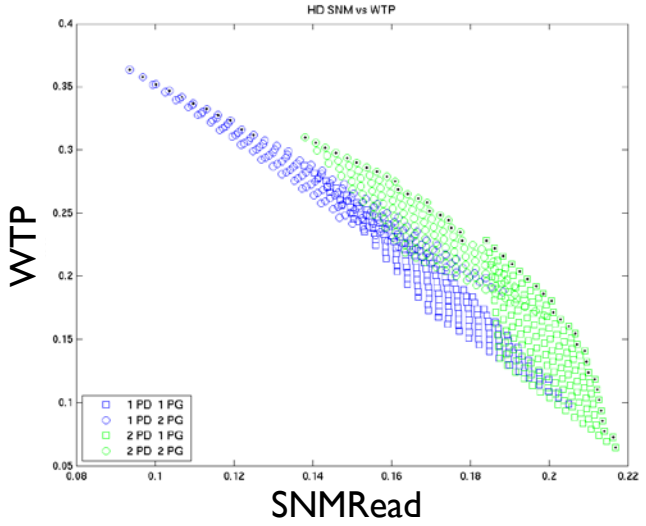


SRAM CELL DESIGN SPACE: FINFET SOI CELL (VDD=0.8V)

High Density Low Power (HDLP)

Area < 0.017 um2





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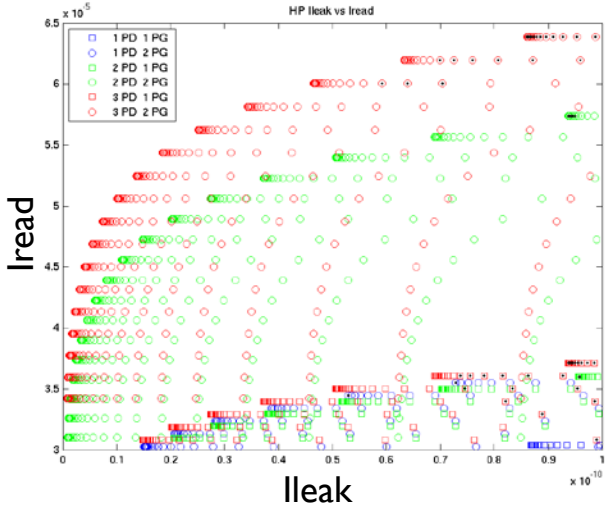

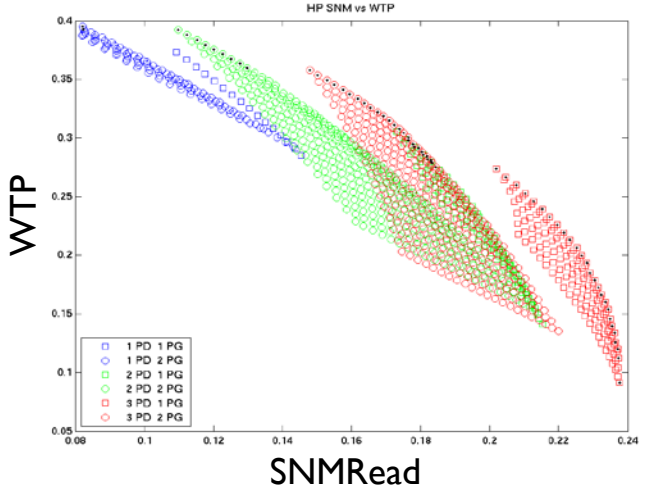

NOMINAL CHARACTERISTICS OF SELECTED SRAM CELL DESIGNS

	Planar Vdd=1V		FinFET Vdd=0.8V		
	HDLP	HP	HD (1/1/1)*	HD (1/2/2)*	HP (1/2/3)*
Area (um^2)	0.017	0.019	0.0145	0.017	0.019
I_read (uA)	16.56	26.01	22.79	37.37	60.06
I_leak (pA)	19.29	31.10	8.09	5.98	70.41
SNMR (mV)	200.1	202.6	167.2	177.9	184.4
SNMH (mV)	390.2	410.5	353.5	350.2	344.0
WTP (mV)	308.0	326.0	220.3	228.4	275.2
L (nm)	16	16	10	10	10
PDW (nm)	30	45	30	60	90
PGW (nm)	20	35	30	60	60
PUW (nm)	20	20	30	30	30
Device Type	HVT				
dVt(n) (mV)	+170	+230	0	+50	-40
dVt(p) (mV)	-160	-70	0	+10	+70

(*) x/y/z = #x fin pull up/ #y fins pass gate/#z fins pull down

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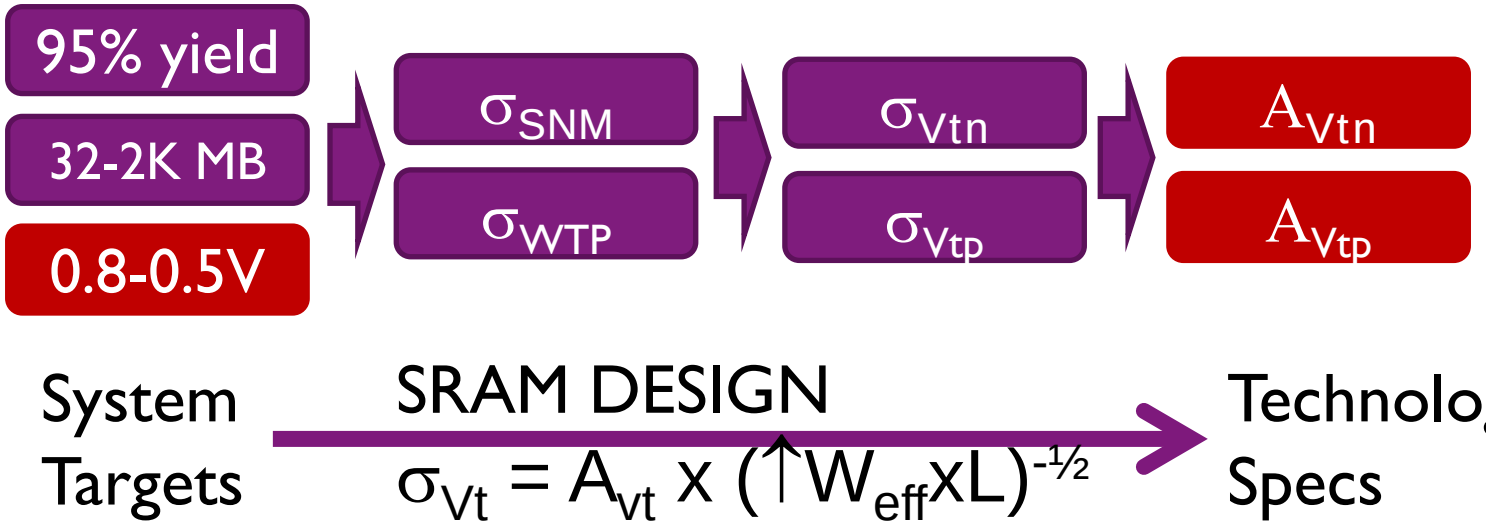
CONCLUSIONS

YIELD CONSIDERATIONS: SCALING TARGETS FOR AVT

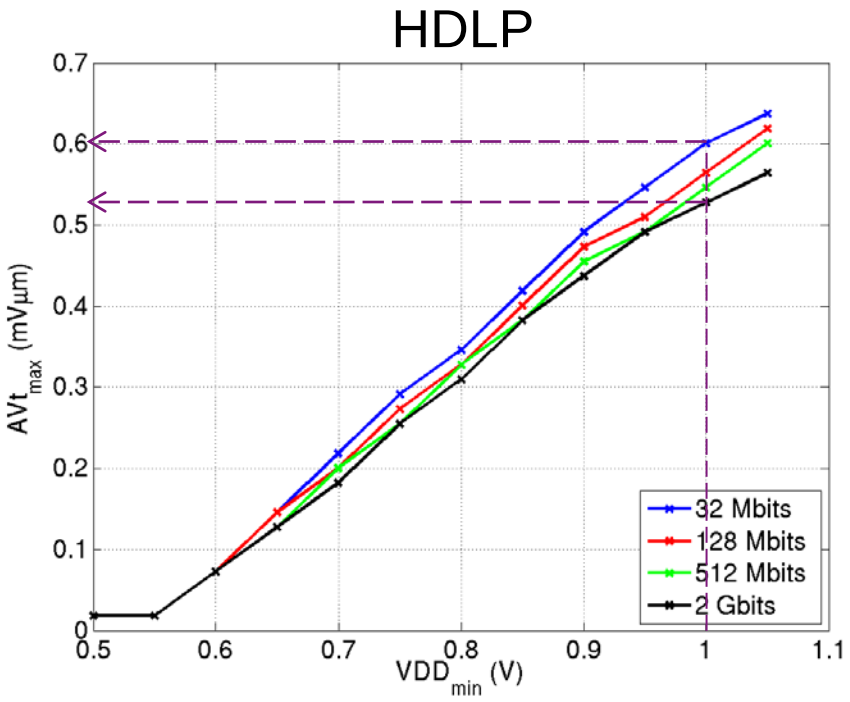
- "Plain vanilla" 6T SRAM cell - no additional assist circuit techniques
- Stability yield (mismatch) > 95%
- Aggressive array size targets: 32MB – 2 GB
  - Today:
    - Intel i7 quad-core: 8MB (shared cache)
    - Eg. Qualcomm's (snapdragon) MSM8974 28nm Quad-core: 2MB (shared cache)
- Supply Voltages under analysis:

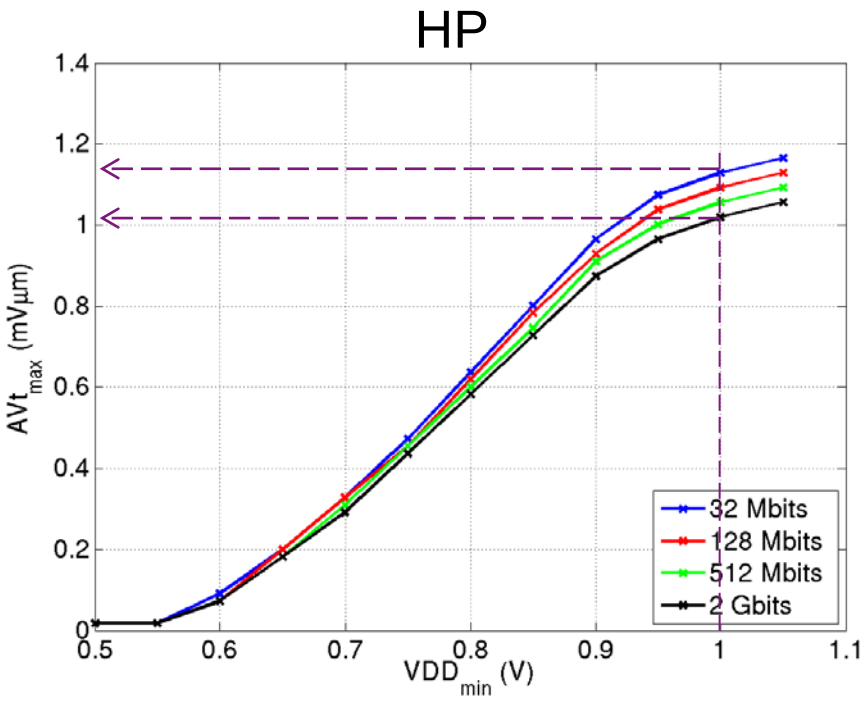
  0.8V ... 0.7V ... 0.6V ... 0.5V
- Technology Node: 10nm

YIELD CONSIDERATIONS: SCALING TARGETS FOR AVT



AVT/VDDMIN ANALYSIS FOR ACCESS STABILITY FOR THE SELECTED PLANAR CELLS



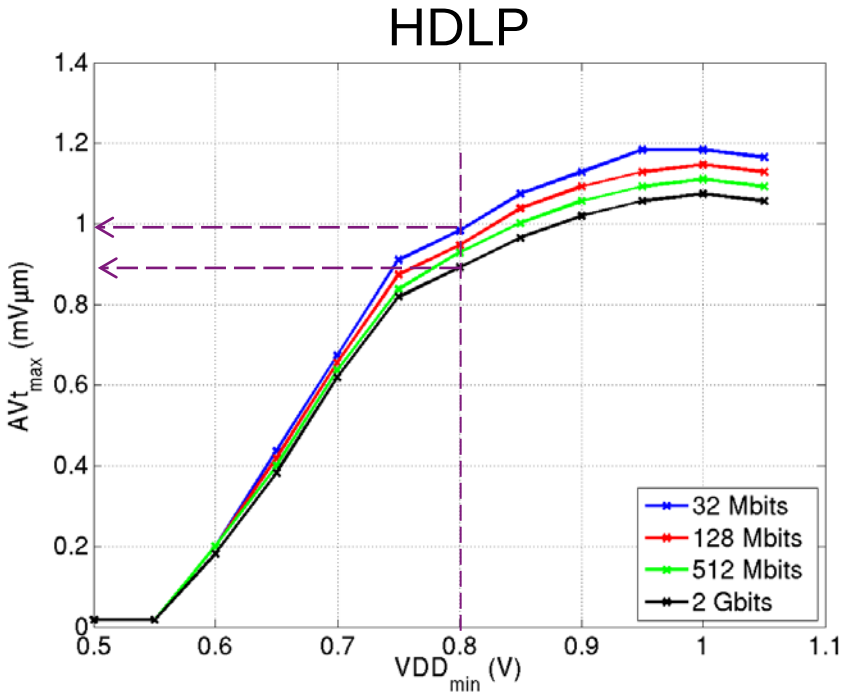


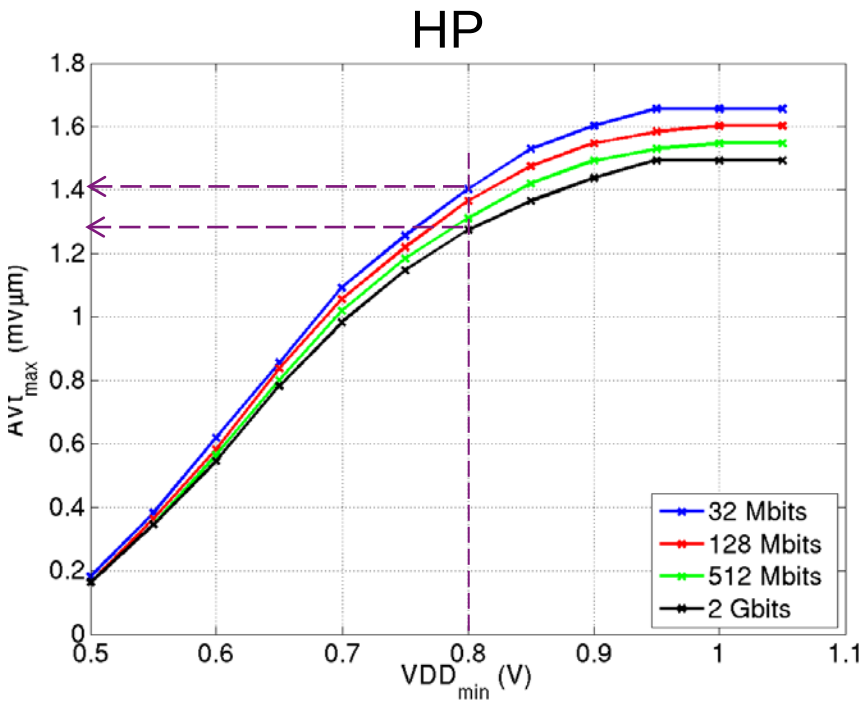
Minimum achievable AVt for bulk planar: 1.5 mVμm

Minimum required AVt for planar SRAM:

- **HDLP: 0.52-0.6 mVμm: NOT OK**
- **HP: 1.0-1.15 mVμm: NOT OK**

AVT/VDDMIN ANALYSIS FOR ACCESS STABILITY FOR THE SELECTED SOIFF CELLS (1/2/2 FIN)





Minimum achievable AVt for SOIFF: 0.8 mVμm

Minimum required AVt for SOIFF SRAM:

- **HDLP: 0.9-1.0 mVμm: OK!**
- **HP: 1.25-1.4 mVμm: OK!**

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SUMMARY

Methodology in place (TRAMS year 1):

- Automated environment ready for sensitivity analysis:
  - from device measurement to SRAM cell
  - From SRAM cell to SRAM array

"Apple to apple" comparison between planar and FinFET: area, stability metrics, process assumptions

Symbolic layout analysis for high-level area model

Planar SRAM @10nm:

- Incapable of meeting targets below for Vdd below 1.0V
- Unstable cell even at 1.0V

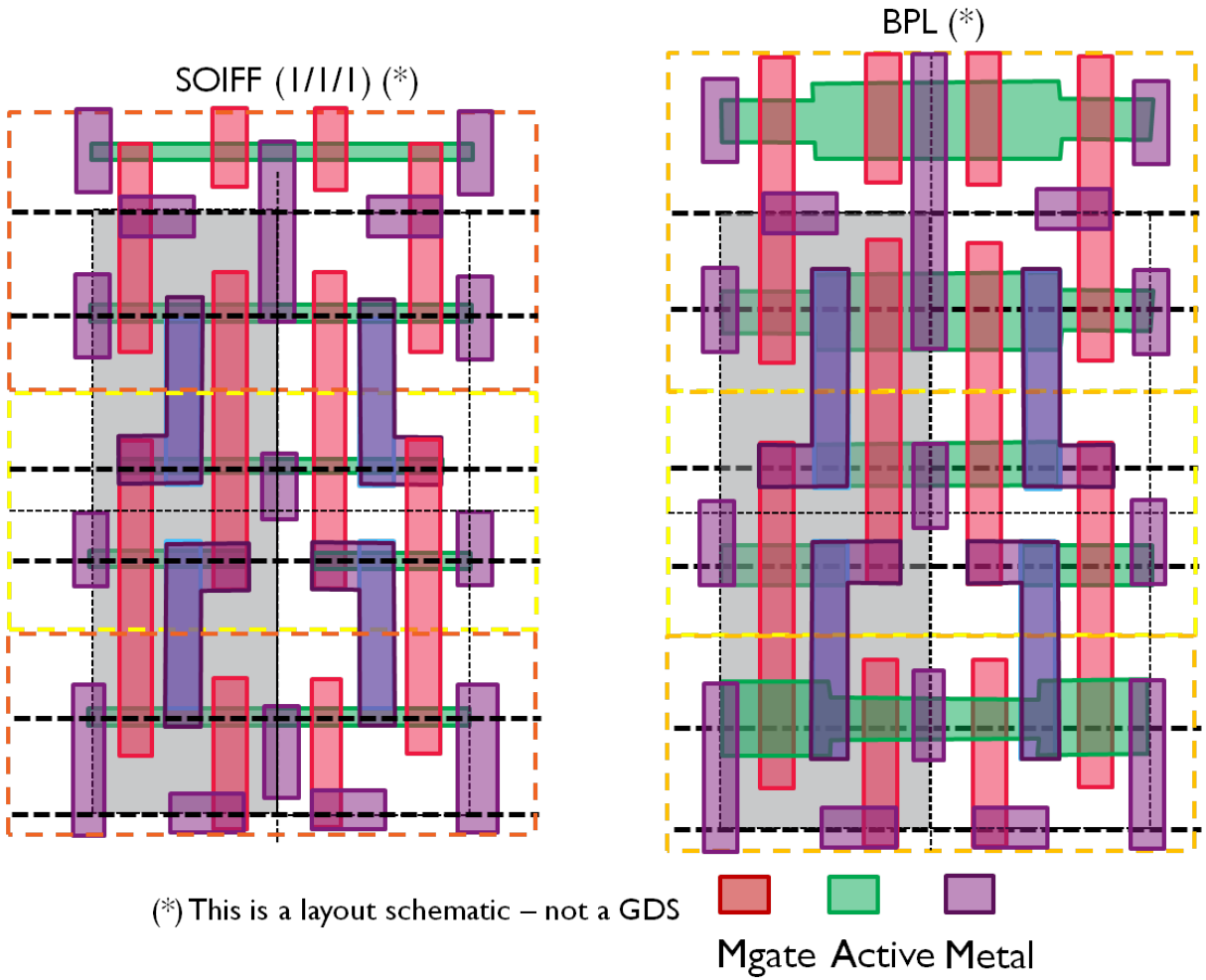
SOIFinFET @10nm:

- Meets targtes at 0.8V
- Stable cell operation at 0.8V (and below)
- Requires multi-fin configuration: 1/2/2

THANK YOU!

BACK-UP SLIDES

SINGLE-FIN FIN FENT AND PLANAR CELL ARCHITECTURES



CELL ARCHITECTURE OPTIONS FOR MLTI-FIN FINFET SRAM CELL CONFIGURATIONS